LISTING OF THE CLAIMS

1. (Currently Amended) A method of forming a doped gate structure on a semiconductor device, comprising the steps:

providing a semiconductor device including a substrate and a gate dielectric layer on said substrate;

forming a gate stack on said dielectric layer, including the steps of

forming a first gate layer on the dielectric layer, and

forming a second gate layer on top of the first gate layer;

forming a spacer around the first and second layers;

removing the second layer; ~~and~~

~~implanting~~ performing an ion implantation step to implant ions in the first gate layer ~~by directing said ions directly into said first gate layer~~ to form a doped gate above the gate dielectric layer; and

keeping the ions used in said ion implantation step, away from said substrate, including the step of using said spacer, during the ~~implanting~~ implantation step, to ~~mark~~ mask said substrate from the ions used in said ~~implanting~~ implantation step.

2. (Previously Presented) A method according to Claim 1, wherein the spacer is a first spacer, and further comprising the steps of:

removing the first spacer;

forming a second spacer, thinner than the first spacer, around the first gate layer; and

implanting further ions in the semiconductor device, around the second spacer, to form source and drain extension regions in the semiconductor device, around the second spacer.

3. (Original) A method according to Claim 2, wherein the step of removing the first spacer occurs after the step of implanting ions in the first gate layer.

4. (Previously Presented) A method according to Claim 2, further comprising the step of:

forming a third spacer around the first gate layer and above the source and drain extension regions.

5. (Currently Amended) A method of forming a doped gate structure on a semiconductor device, comprising the steps:

providing a semiconductor device including a substrate and a gate dielectric layer on said substrate;

forming a gate stack on said dielectric layer, including the steps of

forming a first gate layer on the dielectric layer, and

forming a second gate layer on top of the first gate layer;

forming a spacer around the first and second layers;

removing the second layer; and

~~implanting~~ performing an ion implantation step to implant ions in the first gate layer ~~by directing said ions directly into said first gate layer~~ to form a doped gate above the gate dielectric layer; and

keeping the ions used in said ion implantation step, away from said substrate, including the step of using said spacer, during the ~~implanting~~ implantation step, to mask said substrate from the ions used in said ~~implanting~~ implantation step; wherein:

the first gate layer is comprised of polysilicon; and

the second layer is comprised of polygermanium.

6. (Original) A method according to Claim 1, wherein the spacer is comprised of silicon oxide.

7. (Original) A method according to Claim 1, wherein:

the first gate layer has a height of about 150 nm; and

the second layer has a height of about 150 nm.

8. (Previously Presented) A method of fabricating a semiconductor device, comprising the steps:

providing a semiconductor substrate;

forming a gate dielectric layer on the substrate;

forming a gate stack on said dielectric layer, including the steps of

i) forming a first gate layer on the dielectric layer, and

ii) forming a second gate layer on the first gate layer;

forming a first spacer around the gate stack;

removing the second gate layer,

implanting ions in the first gate layer to form a doped gate above the gate dielectric layer;

after the step of implanting ions in the first gate layer,

removing the first spacer,

forming a second spacer, thinner than the first spacer, around the first gate layer, and

implanting further ions in the semiconductor device, around the second spacer, to form doped source and drain extension regions in the semiconductor device

9. (Currently Amended) A method according to Claim 8, comprising the further step of:

forming a third spacer around the gate stack and above the source and drain extension regions ~~extensions~~.

10. (Original) A method according to Claim 8, wherein each of the first gate layer and second gate layer has a height of about 150 nm.

11. (Original) A method according to Claim 8, wherein the first gate layer is comprised of polysilicon.

12. (Original) A method according to Claim 8, wherein the first spacer is comprised of silicon oxide.

13. (Withdrawn) A semiconductor structure, comprising:

a substrate including a gate dielectric layer;

a gate stack on the gate dielectric layer, said gate stack including a first gate layer on the dielectric layer and comprised of a first material, and a second layer on top of the first gate layer and comprised of a second material different than the first material; and

a disposable spacer extending around the gate stack, and extending upward above the substrate to a level higher than the top of the first gate layer.

14. (Withdrawn) A semiconductor structure according to Claim 13, wherein the disposable spacer thickness is equal or thicker than the first gate layer so that at least 2x fatter spacer is formed.

15. (Withdrawn) A semiconductor structure according to Claim 13, wherein the spacer extends upward substantially to the top of the gate stack.

16. (Withdrawn) A semiconductor structure according to Claim 13, further comprising a liner deposited on the gate stack between the gate stack and the spacer.

17. (Withdrawn) A semiconductor structure according to Claim 16, wherein said liner is also deposited on the semiconductor substrate, between said substrate and the spacer.

18. (Currently Amended) A method according to Claim 1, wherein the ~~implanting~~ step of performing an ion implantation includes the step of implanting said ions in the first gate layer while keeping the spacer around the first gate layer.